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3-Bit R-2R Digital to Analog Converter Using Binary and Thermometer Code

Vishva Patel[*1], Rajanikant Soni[2]

[*1] PG Student, Gujarat Technology University, Electronics and Communication, LCIT-Bhandu, Mehsana, Gujarat, India

[2] Assistant Professor. Electronics and Communication, LCIT-Bhandu, Mehsana, Gujarat, India

patelvishva222@gmail.com

Abstract

In this paper analysis of 3-bit R-2r ladder DAC designed with the specification of INL &DNL .The simulation & analysis is done using the binary and thermometer code. In this design DAC the Maximum INL & DNL is 0.15 achieved . The circuit simulation is done using the Eldo Spice in Mentor Graphics Tool with the 180nm CMOS process Technology.

Keywords: Digital to analog (DAC), Differential Nonlinearity (DNL), Integral Nonlinearity (INL), R-2R ladder network

Introduction

Among the most popular architectures are DACs based on resistor ladders and current steering. These architectures are very well suited for implementation in standard occupied area ,power consumption and speed. In general requiring N-bit DAC resolution implies. Achieving an error of less than 0.5LSB depending on DAC architecture . This translates to a maximum error of the MSB value (current or resistance). The some circuit performance of the designed circuit is improved. In ordered to validate circuit performance, the designed R-2R DAC has been simulated in eldo spice tool of Mentor Graphics using model parameter for 180nm CMOS process. The results shows that INL and DNL of the designed circuit.

The remaining of this paper is organized in the following section, a basic concept of R-2R ladder network II. Next a modification of CMOS EQUIVALENT Binary circuit of R-2R DAC in section III. CMOS EQUIVALENT Binary circuit of R-2R DAC in section IV. In addition, simulated results of the R-2R DAC and conclusion are presented in section V and VI respectively.

Basic Concept of R-2R Ladder Network

The R-2R ladder consists of two different resistors placed in a configuration as shown in fig 1. The inputs to the ladder are fed from a N-bit inputs . The input voltages range from 0V to 2V. Here R- 2R network is also converted in to the CMOS equivalent circuits. This configuration consists of a network of resistors alternating in value of Rand 2R.Starting at the right end of the network, notice that the resistance looking to the right of any node to ground is 2R.Each node voltage is related to Vref,by a binary-weighted relationship caused by the voltage division of the ladder network. The total current flowing from Vref is constant, since the potential at the bottom of each switched resistor is always zero volts. Therefore, the node voltages will remain constant for any value of the digital input.The output voltage, Vout' is determined by the equation 1.where D indicate the digital input word decimal value, n indicate DAC resolution, and DAC reference voltage is Vref.

$$V_{out} = D\left(\frac{V_{ref}}{2^n}\right) \quad (1)$$

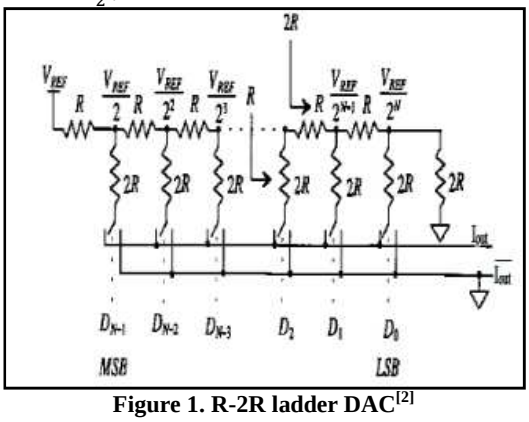

Figure 1. R-2R ladder DAC[2]

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Cmos Equivalent Binary Circuit of r-2r dac

An example of a 3 -bit R-2R MOS converter is shown in Figure2.In this figure R-2R cell shown with a possible Combination with the bit current switch. All transistors in this system are equal. Depending upon the input current 2I, transistor M1 and M2 divide the input current 2I. Transistors M1 and M2 can operate in saturated mode or in a triode mode. In saturated mode transistors M1 and M2 divide the input currents 2I in to two equal currents I. In this case transistor M3 acts as a cascade transistor and supplies the output currents to the load. At the moments transistors m1 and M2 are in triode region, then these transistors can be seen as a resistor with value R. In this case transistor M3 performs an equal resistor of value R. In this way R-2R network is implemented and with careful termination an accurate binary weighted current division is obtained .However it is possible to include the switches in to the network by adding transistor M4.at the moment data is high, then transistor M3 is used in the network as described before and the output current Iout = I1 is supplied to the load . At the moment data bar is high, then transistor M4 is used in the network as described before and the output current Iout Bar = I2 is supplied to the load. By cascading method the basic elements of 3-bit converter can be designed as shown in figure 2. The transistor system can be scaled depending upon the current value owing through the individual stages. In this system trail current 8I is divided by 4I, 2I, I and I. The extra current I is obtained in the last stage Is supplied to the bias voltage and it is not required for the digital to analog converter. With large size of the division transistor, it is possible to obtain 10 bit resolution with +/-0.5 linearity. An accurate switching of the current is required to obtain a small glitch when the digital to analog converter is switched around the MSB values .in the offset binary coded converter system. Timing is very important here. Biggest problem in R-2R DAC is mismatching of resisters values. This creates error in resolution. Resolution can be achieved by using operation amplifier or Low pass filter as a next stage. Proper switching is also very important. Biggest problem in R-2R DAC is mismatching of resisters values. This creates error in resolution. Resolution can be achieved by using operation amplifier or Low pass filter as a next stage. Proper switching is also very important.

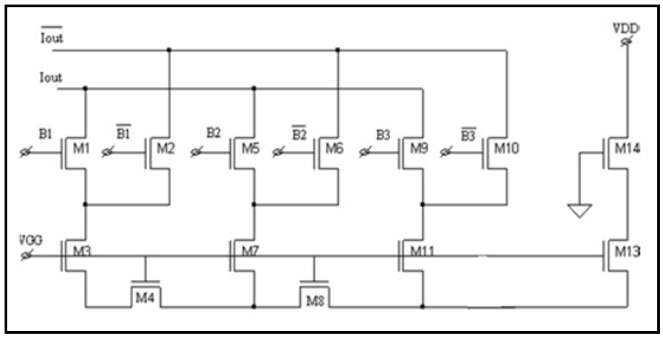

Figure 2. CMOS equivalent circuit of 3-bit R-2R DAC

Then to calculate the value of Resister related to different parameter is follows, The resistance of a MOSFET operated in the linear mode is given by:

$$R = \frac{V_{DS}}{I_D} \qquad (2)$$

Where, V_{DS}=drain-source voltage, I_D=drain-current

The drain-source voltage and the drain current are related by:

$$I_D = \mu . c_{ox} X \left(\frac{W}{L}\right) X (V_{gs} - V_t) X V_{ds} \quad \text{for} \quad V_{ds} < (V_{gs} - V_t) \quad (3)$$

Cmos Equivalent Circuit for Thermometer r-2r dac

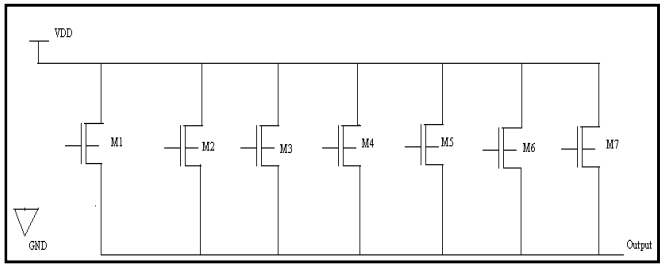

Figure 3. R2R Schematic for Thermometer code .

Thermometer coding is one approach to representing information that is to be presented to an artificial neural network. Thermometer coding is usually used to represent a quantitative variable. Imagine some variable of this type that varies in value from 0 to 10. Thermometer code will be all 1's from the LSB up to the value of k'th bit, D_k and all 0's above it .the point at which the input code changes from all 1's to all 0's "floats" up or down and resembles the action of a thermometer ,hence the name.

Simulation Result

The designed R-2R is simulated by using eldo spice for 180nm CMOS process parameter. By applying input volts=2 V as a pulse and digital input

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from 000 to 111 for three bit we achieved respective voltage as shown in figure 4 and figure 5 and observe respective parameters like INL,DNL,Offset,etc.

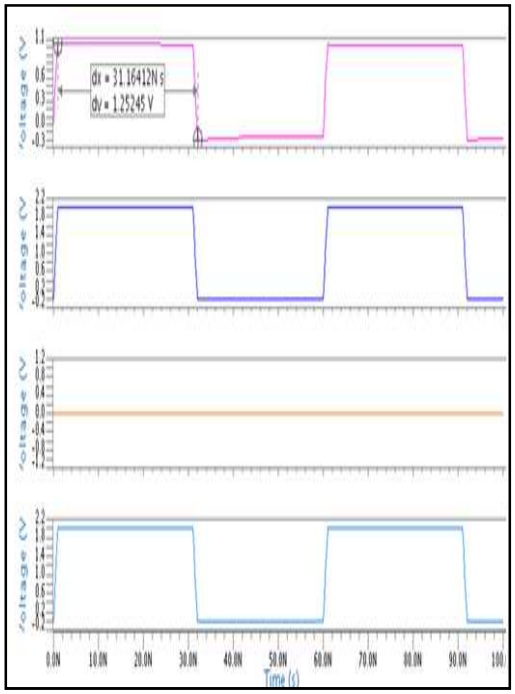

Figure 4. input 101 and output 1.25 V for binary R-2R DAC

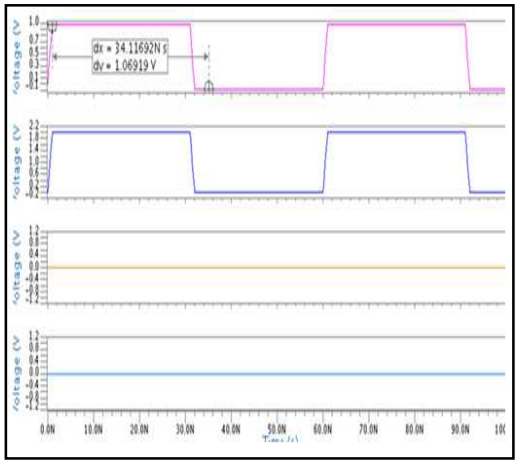

Figure 5. input 100 and output 1.06 V for binary R-2R DAC

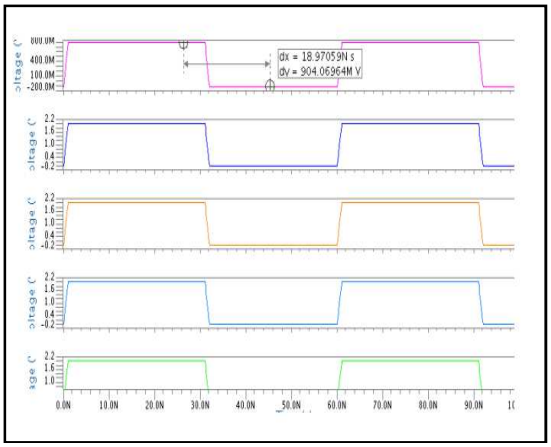

Figure 6. input 0001111 and output .94V for Thermometer DAC

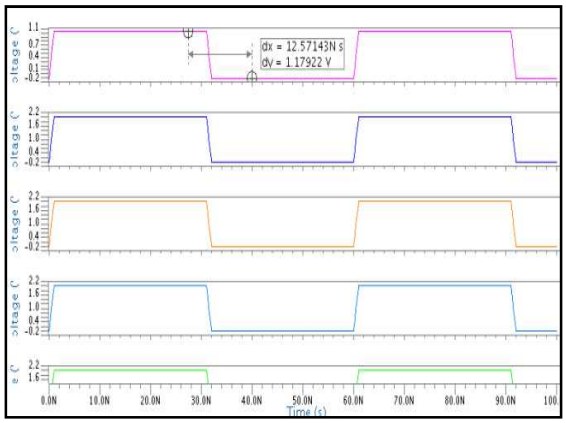

Figure 7. input 0011111 and output 1.17V for Thermometer DAC

A Integral Non-Linearity

INL= Output value for input code n - Output value of the reference line at that point.

For 3 bit R-2R DAC input bits are from 000 to 111. The respective Table I presentation for 3 bit binary R-2R ladder with technology 180nm is as follow and from the above graph we find that maximum INL for 180nm is 0.15.

Table II presentation for 3 bit Thermometer R-2R DAC with technology 180nm is as follow and from the above graph we find that maximum INL for 180nm is 0.15 .

Table I INL for 3bit Binary R-2R DAC

input	ideal o/p	actual o/p	different
000	0.00	0.00	0.00
001	0.25	0.35	0.10
010	0.50	0.65	0.15
011	0.75	0.85	0.10
100	1.00	1.15	0.05
101	1.25	1.30	0.05
110	1.50	1.60	0.10
111	1.75	1.83	0.08

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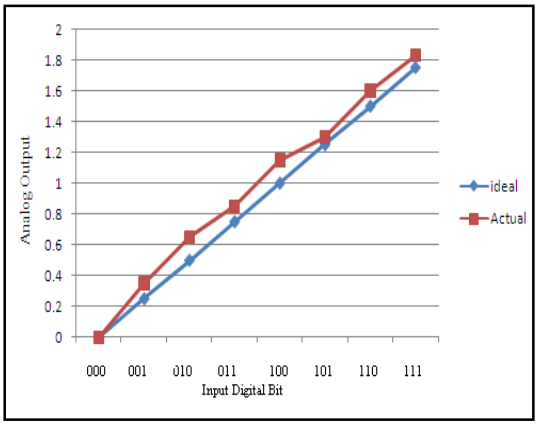

Figure 8. INL for 3bit Binary R-2R DAC

Table II INL for 3bit Thermometer R-2R DAC

input	ideal o/p	actual o/p	different
0000000	0.00	0.00	0.00
0000001	0.25	0.13	0.12
0000011	0.50	0. 37	0.13
0000111	0.75	0.60	0.15
0001111	1.00	0.90	0.1
0011111	1.25	1.17	0.05
0111111	1.50	1.53	0.03
1111111	1.75	1.78	0.03

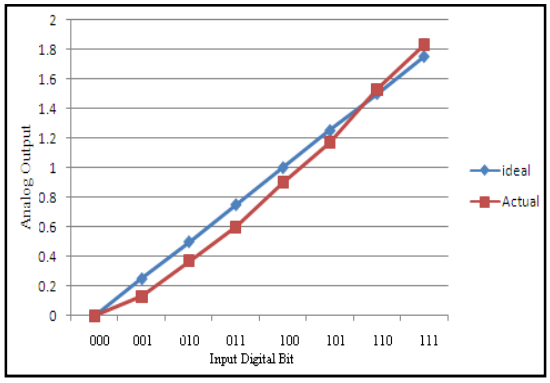

Figure 9. INL for 3bit Thermometer R-2R DAC

B Differential Non-Linearity

DNL=Actual incremental height of transition n – Ideal increment height.

For 3 bit R-2R DAC input bits are from 000 to 11. And y axis of figure 10 shows ideal and actual DNL. And the respective Table III presentation for 3-bit R-2R ladder with technology 180 nm is allow and from the above graph we find that Maximum DNL for 180nm is 0.15

Table IV presentation for 3-bit Thermometer R-2R DAC with technology 180 nm is allow and from the above graph we find that Maximum DNL for 180nm is 0.15

Table III DNL for 3bit Binary R-2R DAC

input	ideal o/p	actual o/p	different
000	0.00	0.00	0.00
001	0.25	0.35	0.10
010	0.50	0.65	0.15
011	0.75	0.85	0.10
100	1.00	1.15	0.05
101	1.25	1.30	0.05
110	1.50	1.60	0.10
111	1.75	1.83	0.08

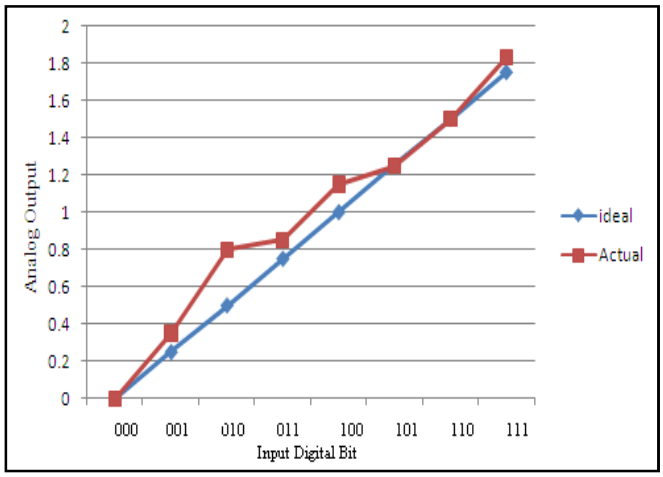

Figure 10. DNL for 3bit Binary R-2R DAC

Table IV DNL for 3bit Thermometer R-2R DAC

input	ideal o/p	actual o/p	different
0000000	0.00	0.00	0.00
0000001	0.25	0.13	0.10
0000011	0.50	0. 37	0.15
0000111	0.75	0.60	0.10
0001111	1.00	0.90	0.05
0011111	1.25	1.17	0.05
0111111	1.50	1.53	0.10
1111111	1.75	1.78	0.03

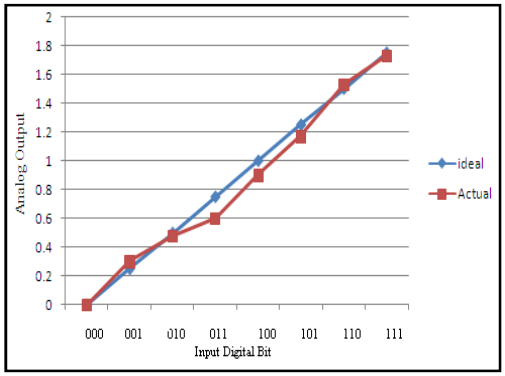

Figure 11. DNL for 3bit Thermometer R-2R DAC

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Conclusion

In this paper 3 Bit Binary and Thermometer DAC simulated in 180nm technology. In my simulation result INL,DNL and power dissipation is Improve. Thermometer architecture is not use for higher bit. Its beneficial for low bit DAC.

Table V. Different measured parameter in 180nm for 3 bit Binary & Thermometer R-2R DAC

Parameter	Binary R-2R DAC	Thermometer R-2R DAC
Bit	3	3
INL MAX	0.15	0.15
DNL MAX	0.15	0.15
Technology	180nm	180nm
Power supply(V)	2	2
Power dissipation(µW)	539.76	212.20

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